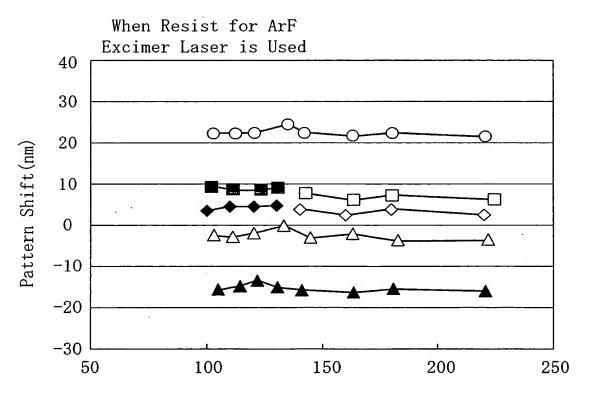


FIG. 1

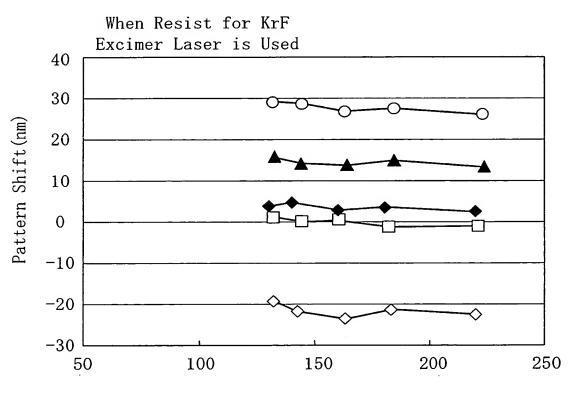
Condition A (no tilting occurs)
Condition A (tilting occurs)
Condition B (no tilting occurs)
Condition C (no tilting occurs)
Condition C (tilting occurs)
Condition D (no tilting occurs)
Condition E (no tilting occurs)



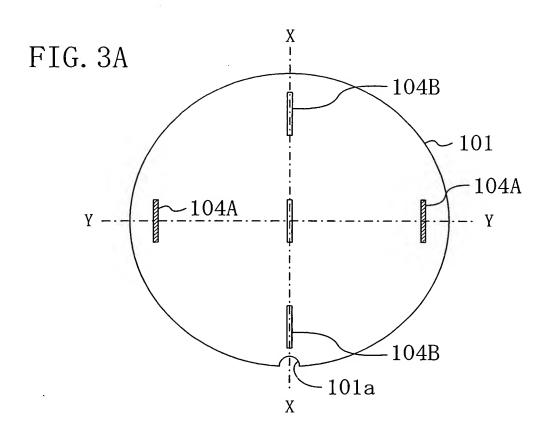
Initial Value of Resist Pattern Size(nm)

FIG. 2

Condition 1 (no tilting occurs)
Condition 2 (no tilting occurs)
Condition 3 (no tilting occurs)
Condition 4 (no tilting occurs)
Condition 5 (no tilting occurs)



Initial Value of Resist Pattern Size(nm)



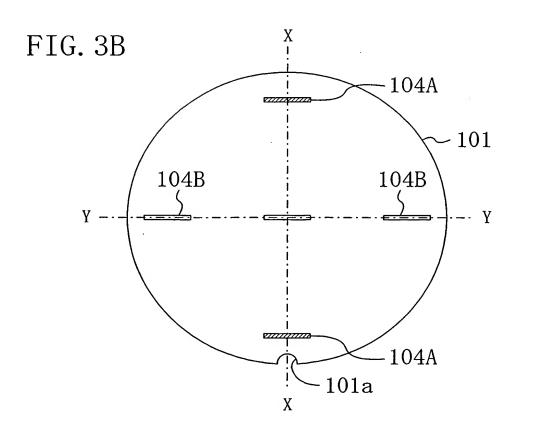


FIG. 4A

FIG. 4C

- 108

105

104

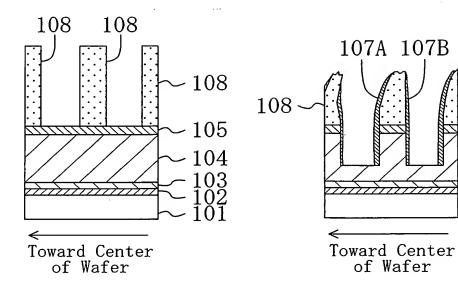


FIG. 4B

FIG. 4D

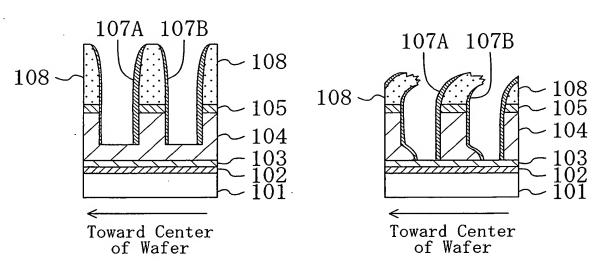


FIG. 5C FIG. 5A 108 108 107A 107B - 108 - 108 108 105 104 - 105 - 104 $103 \\ 102 \\ 101$ Toward Center of Wafer Toward Center of Wafer FIG. 5D FIG. 5B 107A 107B 107A 107B 108 108 - 108 108 105 105 104 104

Toward Center of Wafer

Toward Center of Wafer

FIG. 6A

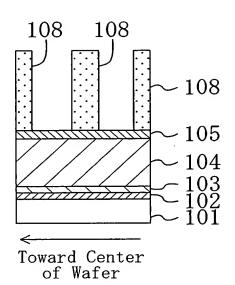


FIG. 6C

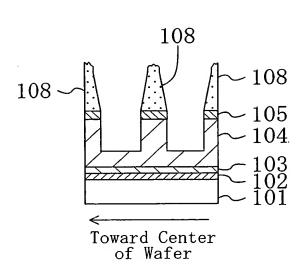


FIG. 6B

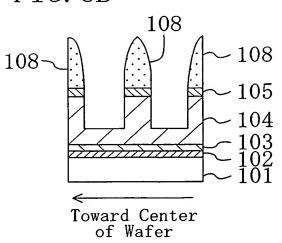
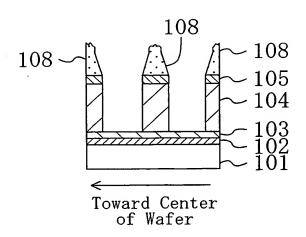


FIG. 6D



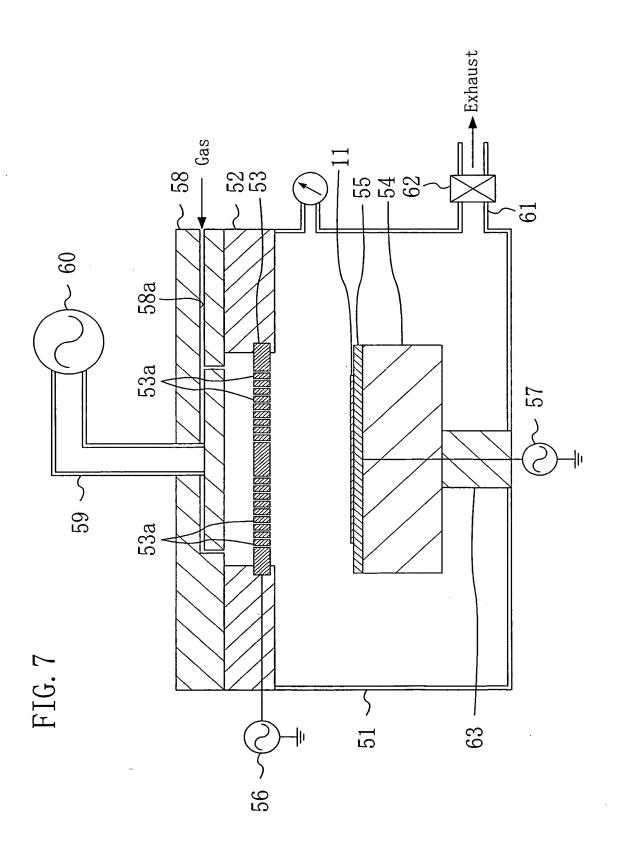


FIG. 8A

16A

15

14

13

12

11

Toward Center
of Wafer

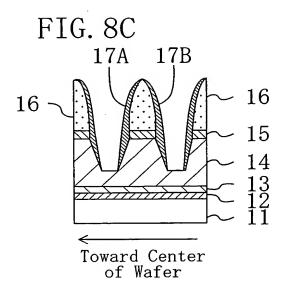


FIG. 8B

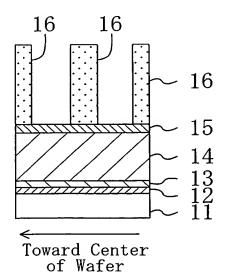


FIG. 8D

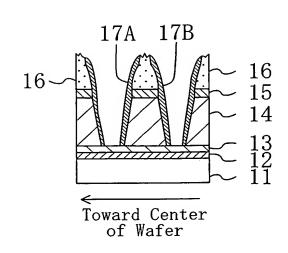


FIG. 9A

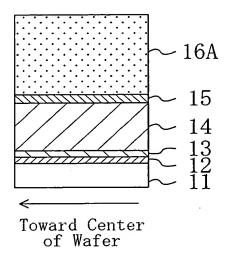


FIG. 9C

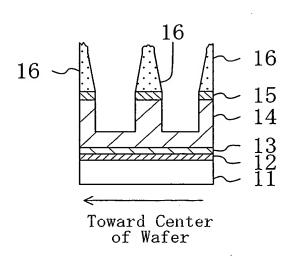


FIG. 9B

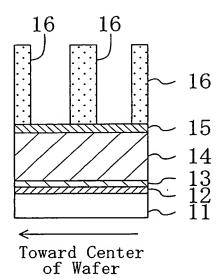


FIG. 9D

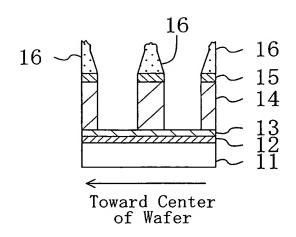


FIG. 10A

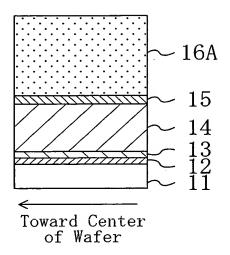


FIG. 10C

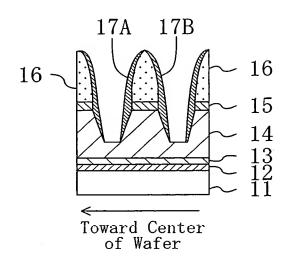


FIG. 10B

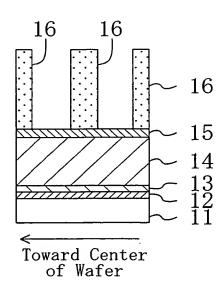
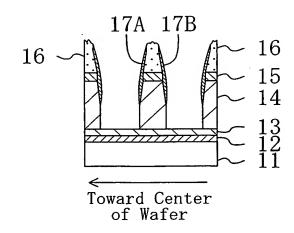


FIG. 10D



11/11 FIG. 11A PRIOR ART - 104 103 102 101 Toward Center of Wafer FIG. 11B PRIOR ART $\sim 106A$ -105- 104 Toward Center of Wafer

FIG. 11C PRIOR ART

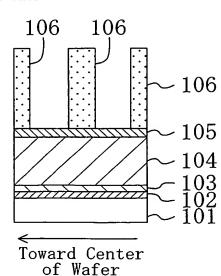
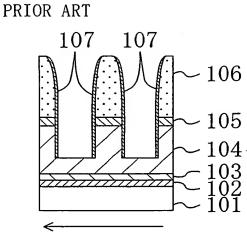
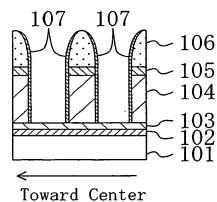


FIG. 11D



Toward Center of Wafer

FIG. 11E PRIOR ART



of Wafer